NBSIR 81-2319

Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened Charge-Coupled Device (CCD) Imagers: Annual Report, May 15, 1980 to May 14, 1981

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
Center for Electronics and Electrical Engineering
Electron Devices Division
Washington, DC 20234

August 1981

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e Charles Stark Draper Laboratory, Inc.
mbridge, MA 02139

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DEVELOPMENT OF TEST STRUCTURES FOR CHARACTERIZATION OF THE FABRICATION AND PERFORMANCE OF RADIATION-HARDENED CHARGE-COUPLED DEVICE (CCD) IMAGERS: ANNUAL REPORT, MAY 15, 1980 TO MAY 14, 1981

G. P. Carver

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened Charge-Coupled Device (CCD) Imagers: Annual Report, May 15, 1980 to May 14, 1981

by

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The purpose of this project is to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. During the period covered by this report, consultation was provided to The Charles Stark Draper Laboratory, Inc. (CSDL) and to CSDL contractors on the implementation and use of test structures developed previously during this project. In addition, the results of measurements on CCD imager wafers using the surface-channel and buried-channel, integrated gated-diode electrometers, before and after exposure to ^{60}Co radiation, and using the cross bridge/electrical alignment test structures are reported. Examples of cross sections of the CCDs made by beveling and staining are also presented.

Key words: CCD; cross-bridge sheet resistor; electrical alignment test structure; gated diode; integrated gated-diode electrometer; integrated test structure; MOSFET dc profiler; test structure.

1. INTRODUCTION

This report describes work performed for The Charles Stark Draper Laboratory, Inc. (CSDL) under CSDL Prime Contract N00030-79-0096 issued by the Department of the Navy, Strategic Systems Project Office, for the period beginning May 15, 1980 and ending May 14, 1981. This work constitutes a program entitled "Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened CCD Imagers." The present program is a continuation of activities initiated in FY-1978.

2. OBJECTIVE

This project is intended to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. The goals are to develop the tools which enable CCD manufacturers to measure critical device and process parameters and which provide the end users with information based upon measurements which accurately characterize critical CCD performance. In addition, the test structures and test methods developed are directed at minimizing the hardware and software required to implement fully a suitable test program at CCD manufacturing facilities.

3. SUMMARY OF WORK COMPLETED PRIOR TO THIS REPORTING PERIOD

Designs and specifications for production-compatible test structures useful for the characterization of radiation-hardened CCD imagers were provided [1]. Included in the set of test structures were two devices which had been developed and analyzed in this program, the integrated gated-diode electrometer [2] and the MOSFET dc profiler [3-5]. Interactions with CSDL contractors resulted in successful implementation of the most appropriate test structures. These test structures were used to provide data to meet needs arising from contractors' activities and from CSDL requests [6].

4. RESULTS OF WORK DURING THIS REPORTING PERIOD

Use of the test structures on contractor-fabricated CCD imager chips continued during this period and enabled NBS to provide valuable test information necessary for key decisions by CSDL and the contractors. In addition, preliminary tests were completed on test structures exposed to gamma radiation. As in earlier periods, a variety of technical efforts and consultations were carried out to meet needs arising from contractors' activities or from CSDL requests.

4.1 Measurements Using the Integrated Gated-Diode Electrometer

The generation lifetime and the surface recombination velocity were measured [2] on unpackaged chips and on one complete wafer using the four square-shaped integrated gated-diode electrometers contained on the manufacturer's CCD imager chip. These four test structures include two devices whose gates are fabricated from the first level of polysilicon and two whose gates are fabricated from the second polysilicon level. One of each pair is a buried-channel device; that is, there is an implanted layer in the silicon beneath the gate. The four devices, therefore, can be used to investigate each possible type of interface between the two polysilicon levels and the implanted or unimplanted substrate. The devices are numbered as follows:

Device 1:	Surface Channel	Second polysilicon level gate over unimplanted substrate.
Device 2:	Surface Channel	First polysilicon level gate over unimplanted substrate.
Device 3:	Buried Channel	Second polysilicon level gate over implanted substrate.
Device 4:	Buried Channel	First polysilicon level gate over implanted substrate.

The results of the measurements on a wafer containing 23 complete chips are given in tables 1 through 3. The substrate is p-type, with a room temperature resistivity of approximately 30 Ω•cm. The bulk generation lifetimes under the junction correspond to leakage currents in the range from 5 to 10 pA. For a lifetime of 20 μs, the leakage is 24 nA/cm^2.

The n-type implanted layer has a peak dopant density of approximately 5×10^{16} cm^{-3} at a depth of about 100 nm. Because the depletion region in the implanted layer reaches down to the junction before the surface inverts, it

was not possible to determine the generation lifetime under the gates of the buried-channel devices.

These results indicate (a) that the surface recombination velocity is significantly higher for devices having gates formed from the second polysilicon level compared to devices having gates of the first polysilicon level and (b) that the surface recombination velocity is several times higher for buried-channel devices than for surface-channel devices, as expected. In addition, the bulk generation lifetimes under the gates are smaller than those under the junction.

The wafer on which the above results were obtained was diced and the chips mounted in 44-lead packages. Two surface-channel capacitors and the two surface-channel integrated gated-diode electrometers were bonded out and used as test vehicles in a study whose initial objective was to determine the behavior of the test devices after irradiation using a ^{60}Co source.

Measurements were made on the two surface-channel integrated gated-diode electrometers and on the two surface-channel MOS capacitors on the chips before and after exposure to the radiation. The data were analyzed to obtain the bulk generation lifetime, surface recombination velocity, and flatband voltage shift before and after irradiation at 10^4, 10^5, and 10^6 rads. The test devices on only three chips completed the experiment from a total of ten chips that were packaged and bonded.

Difficulties were experienced in the bonding procedure due to the height of the package sidewalls, the large distances between the package bonding posts and the test structures (which are well inside the edges of the chip), and the relatively small size of the test structure bonding pads (which were orginally designed to serve as probe pads). After the first chip was packaged and bonded, the test structures on it were tested. All 15 bonds were found to be electrically sound and the bonded test structures each functioned properly. Upon completion of the packaging and bonding of the other nine chips, only two additional chips had test structures which behaved as expected. The major problem was that the integrated gated-diode electrometers exhibited excessive bulk leakage, rendering them unsuitable for use in the experiment. It is believed that the bonding procedure introduced crystalline damage in the silicon which greatly increased the measured value of the leakage current.

The three irradiated chips are numbered 24, 22, and 44. During the irradiations, the gates of the integrated gated-diode electrometers and the capacitors on Chip 24 were electrically biased at -9 V with respect to the substrate. This bias would be expected to attract holes created in the oxide away from the interface where they would be trapped. The gates on Chip 22 were shorted to the substrate and the gates on Chip 44 were left floating. These two bias conditions were chosen for comparison with the favorably biased situation.

All three chips were irradiated in the NBS water-shielded ^{60}Co source which has a total activity of about 10 kCi. Measurements on the test structures were performed within one hour before and after each irradiation. When

irradiations were performed on different days, the pre-rad measurement was found to be unchanged from the previous day's post-rad measurement.

The results of the measurements are tabulated in tables 4 through 7. Because of the limited number of devices successfully used to obtain data in this experiment, it is difficult to draw definitive conclusions. The surface damage induced by the gamma irradiation appears to be essentially the same whether the gates of the devices were biased negatively, grounded, or left floating with respect to the substrate. Generally, bulk properties do not change except after the maximum dose. Surface leakage increases significantly only after 10^5 rads, but flat-band voltage shifts occur even at the lowest dose of 10^4 rads.

Experience with bonding and measuring the chips for this experiment requires us to modify the procedures for future experiments. Different packages will be used and probing of the devices will replace bonding, except for the gates which must be connected during the radiation exposures. These changes will reduce the number and length of the bonds, and we expect to have a much greater yield of functioning devices for the electrical measurements.

4.2 Measurements Using the MOSFET dc Profiler

The MOSFET dc profiler [3-5] was used to profile four different ion implants for the CCD imagers. The profiler used is a rectangular MOSFET with a channel length of 28 μm. It was fabricated on an *n*-type <111> silicon wafer with nominal room-temperature resistivity of 10 Ω•cm.

The regular fabrication process was interrupted after the channel stop and source/drain diffusion steps were completed. At this time, a thermal oxide approximately 10 nm thick was grown over the wafer; this oxide was masked with a 800-nm thick layer of aluminum everywhere except in the gate oxide regions and in other regions designated for spreading resistance profile measurements. Two wafers were implanted with phosphorus at 140 keV to respective fluences of 1.5×10^{12} and 3×10^{12} cm^{-2}; one wafer was implanted with phosphorus at 50 keV to a fluence of 1.5×10^{12} cm^{-2}; and one wafer was implanted with arsenic at 140 keV to a fluence of 0.75×10^{12} cm^{-2}. The implantations were performed by a CCD manufacturer. After the wafers were returned to NBS, the aluminum was removed by chemical etching and the implants were activated by annealing at 1000°C for 10 min in an oxygen atmosphere and 225 min in a nitrogen atmosphere. The oxide was chemically removed and the normal process sequence was continued. The final gate oxide was approximately 100 nm thick. Both MOSFET dc and spreading-resistance profiling data were obtained. The results compare favorably and have been separately communicated to CSDL.

4.3 Measurements Using the Cross-Bridge/Electrical Alignment Test Structures

Measurements were made on the cross-bridge/electrical alignment test structures (CBEATS) on the wafer used for the radiation tests. The CBEATS can be used to measure the sheet resistance and linewidth of a conducting channel [7] and the local misalignment between the conducting channel photomask level and the contact window photomask level [8,9]. The conducting channels of the

three CBEATS on each chip are formed in the first polysilicon, second polysilicon, and source/drain diffusion layers.

The average sheet resistance results obtained from three chips on the wafer are as follows:

First Polysilicon	176.1 ± 0.5 Ω/□
Second Polysilicon	106.8 ± 0.3 Ω/□
Diffusion	4.81 ± 0.07 Ω/□

The average linewidths measured on the three chips are:

First Polysilicon	16.6 ± 0.3 μm
Second Polysilicon	16.7 ± 0.3 μm
Diffusion	22.2 ± 0.2 μm

The three devices were designed to have the same linewidth. But as expected, due to overetch of the polysilicon and lateral diffusion of the dopant, the polysilicon lines are narrower than the diffusion lines.

The misalignment results on the three chips are not very useful because they only provide the local level-to-level misalignment at three points. Misalignment between photomask levels is characterized by a relative translation and rotation between the two levels which results in different misalignment vectors at different positions on the wafer. However, the maximum magnitudes of the measured misalignment vectors indicate the magnitude of the local misalignment which may occur on the wafer. The maximum measured misalignments are:

First Polysilicon Level - contact window	1.5 μm
Second Polysilicon Level - contact window	0.84 μm
Diffusion - contact window	0.50 μm

On two other wafers, all three CBEATS on each of the 25 chips on the wafers were measured, and the data were analyzed to obtain the average translation, average rotation, average expansion, and residual misalignment vectors. This information was required for a decision regarding the lithography equipment to be used for a new chip design having smaller feature sizes. The tabulated results and the wafer vector maps of the data are shown in figures 1 through 6. A key feature of the data is that the random component of the local misalignment is generally larger than systematic or gross misalignments associated with the average over the whole wafer of the translation, rotation, or expansion between each pair of mask levels. This conclusion is evidenced by the large standard deviation of the means of the translation components and by the large residual vectors in the wafer maps compared to the initial composite vectors before the systematic components were removed.

This result could be due either to relatively large measurement errors, to random site-to-site misalignments occuring on the masks themselves, or to variations in the wafer processing. Examples of processing variations which could lead to apparent misalignments are asymmetric etching of the edges of the contact windows, variations in the sheet resistance within each struc-

ture, or spatial nonuniformities in the contact resistance within the contact windows.

4.4 Beveled and Stained Cross Sections

Several CCDs were beveled and stained to produce a cross-section view in the plane perpendicular to the direction of charge transfer in the channels in the imager array. The purpose of this work was to measure the width of the channel to evaluate the potential for increasing the CCD full well capacity by decreasing the extent of the channel-stop regions. Photographs of the cross sections and information to interpret adequately the details in the photographs were transmitted to CSDL where the analysis was performed. Examples of the cross sections are shown in figures 7 and 8.

5. CONCLUDING REMARKS

During this reporting period, continued understanding of the use of test structures for characterizing the CCD chips and of the measurement procedures was developed. These occurrences were motivated in part by the numerous interactions between NBS and CSDL and the CCD vendors. This report documents only selected examples of the work that was performed and discussed.

Acknowledgments

The assistance of R. L. Mattis and T. J. Russell in using their computer programs to analyze the electrical alignment test structure data and to prepare the vector wafer maps is greatly appreciated.

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Table 1

Bulk Lifetime Under the Junction:* Wafer 30-18

a. Device 1

	29	35	37	33
25	31	35	35	35
23	32	34	34	35
23	28	33	36	32
	25	28	31	29

b. Device 2

	37	42	42	42
31	39	42	44	44
29	39	42	42	42
28	39	42	44	39
	32	31	36	35

c. Device 3

	22	24	24	23
16	23	24	26	26
17	22	24	24	26
17	23	24	24	24
	17	22	24	21

d. Device 4

	30	36	33	30
26	33	33	36	33
27	30	33	36	36
23	33	36	36	36
	27	30	33	27

* Values are given in μs. The positions of the numbers in each array correspond to the positions of the devices on the wafer. The wafer flat is at right.

Table 2

Surface Recombination Velocity:* Wafer 30-18

a. Device 1

	7.6	11.2	7.6	2.7
8.4	7.9	7.9	7.9	12.7
8.4	8.2	7.9	7.9	7.9
7.9	7.6	8.2	7.9	8.5
	8.5	8.5	8.8	8.5

b. Device 2

	4.5	4.2	3.3	4.2
4.2	4.5	3.9	4.2	4.2
4.5	5.4	4.2	4.5	4.2
2.7	4.5	4.2	4.2	4.5
	4.2	7.9	4.2	5.4

c. Device 3

	30	25	25	28
27	28	25	25	25
25	25	25	23	27
25	21	25	23	30
	25	30	28	29

d. Device 4

	22	18	18	15
18	15	18	13	15
25	15	18	18	15
22	9	18	15	15
	9	15	18	15

* Values are given in cm/s. The positions of the numbers in each array correspond to the positions of the devices on the wafer. The wafer flat is at right.

Table 3

Bulk Lifetime Under the Gate:* Wafer 30-18

a. Device 1

	2.0	2.2	2.6	2.5
1.6	2.3	2.2	2.2	2.2
1.7	2.3	2.3	2.3	2.2
1.5	2.1	3.0	2.1	2.1
	1.5	2.9	3.1	2.7

b. Device 2

	4.6	4.3	7.7	7.7
8.2	6.0	4.4	6.4	6.4
5.5	3.7	4.3	8.2	7.7
3.8	4.5	8.2	6.4	3.6
	3.6	6.8	5.0	3.6

* Values are given in μs. The positions of the numbers in each array correspond to the positions of the devices on the wafer. The wafer flat is at right.

Table 4

Lifetime and Leakage Current Density Under the Junction Before and After Irradiation

	Chip 24 (-9 V bias)		Chip 22 (shorted)		Chip 44 (open)	
	Lifetime (μs)	Bulk Leakage Current Density (nA/cm^2)	Lifetime (μs)	Bulk Leakage Current Density (nA/cm^2)	Lifetime (μs)	Bulk Leakage Current Density (nA/cm^2)
Before Irradiation	13	39	12	42	13	39
After 10^4 Rads (Si)	13	39	12	42	13	39
After 10^5 Rads (Si)	13	39	12	42	13	39
After 10^6 Rads (Si)	10	49	11	47	9.5	51

Table 5

Lifetime and Leakage Current Density Under the Gate
Before and After Irradiation*

	Chip 24 (-9 V bias)		Chip 22 (shorted)	
	Lifetime (μs)	Bulk Leakage Current Density (nA/cm^2)	Lifetime (μs)	Bulk Leakage Current Density (nA/cm^2)
Before Irradiation	18	25	22	21
After 10^4 Rads (Si)	18	25	22	21
After 10^5 Rads (Si)	18	25	22	21
After 10^6 Rads (Si)	14	34	12	38

* No data were obtained on Chip 44 because there was excessive current leakage between the gate and the substrate when the gate was biased positive with respect to the substrate.

Table 6

Surface Recombination Velocity for the Polysilicon-2 Gate Oxide

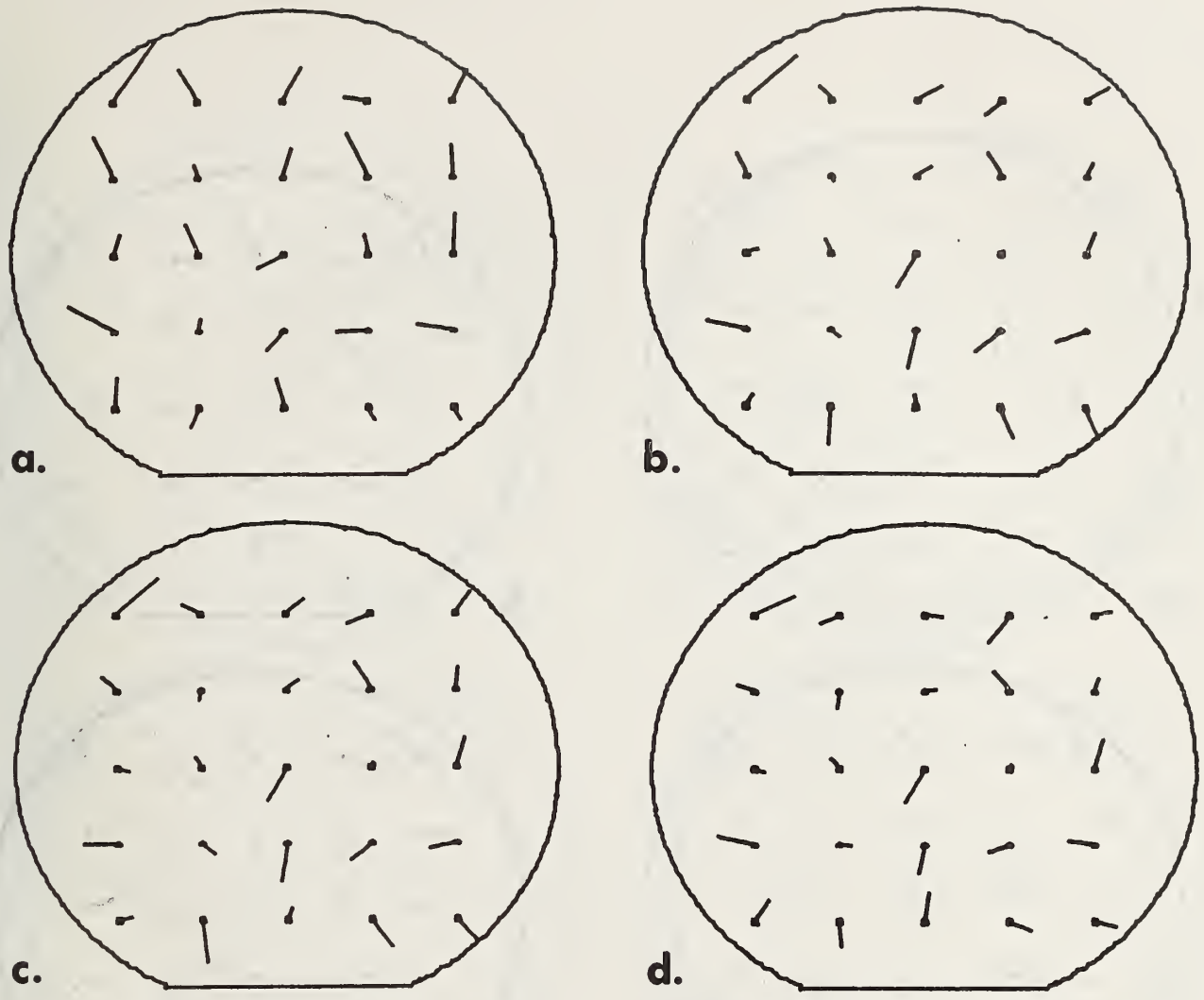
	Chip 24 (-9 V bias)		Chip 22 (shorted)		Chip 44 (open)	
	Surface Recombination Velocity (cm/s)	Surface Leakage Current Density (nA/cm^2)	Surface Recombination Velocity (cm/s)	Surface Leakage Current Density (nA/cm^2)	Surface Recombination Velocity (cm/s)	Surface Leakage Current Density (nA/cm^2)
Before Irradiation	12	15	15	19	11	14
After 10^4 Rads (Si)	12	15	15	19	11	14
After 10^5 Rads (Si)	28	36	28	36	29	38
After 10^6 Rads (Si)	120	157	96	123	120	148

Table 7

Flat-Band Voltage Shifts in Volts

	Chip 24 (-9 V bias)		Chip 22 (shorted)		Chip 44 (open)	
	Polysilicon-1	Polysilicon-2	Polysilicon-1	Polysilicon-2	Polysilicon-1	Polysilicon-2
After 10^4 Rads (Si)	-0.05	-0.06	-0.25	-0.12	-0.0	*
After 10^5 Rads (Si)	-0.55	-0.25	-0.50	-0.25	-0.25	*
After 10^6 Rads (Si)	-1.35	-0.75	-1.50	-0.75	-0.75	*

* No data were obtained because there was excessive current leakage between the gate and the substrate when the gate was biased positive with respect to the substrate.



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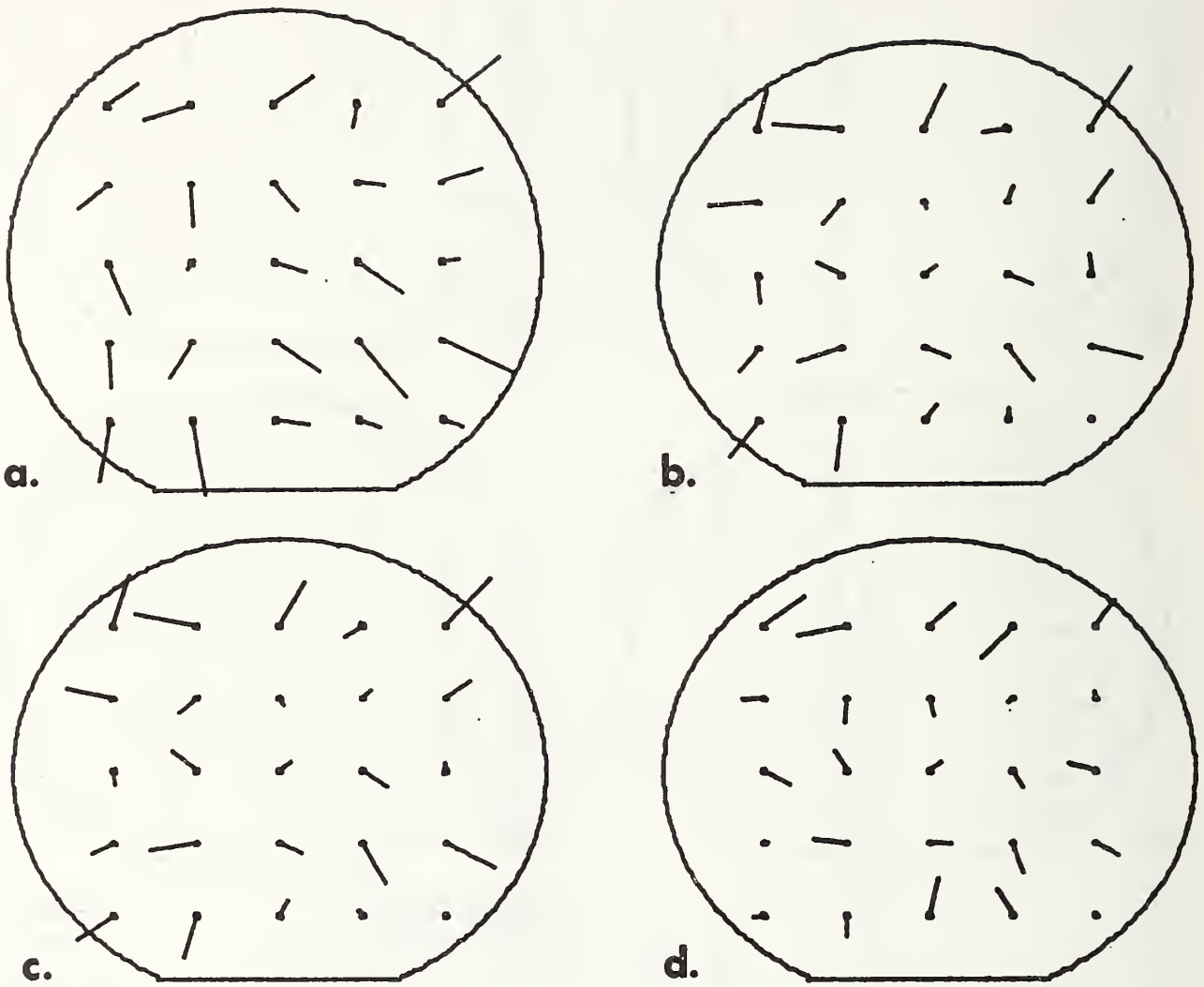
Y TRANSLATION:	0.301
X ANGULAR CONST:	-0.411E+01
Y ANGULAR CONST:	-0.563E+01
X EXPANSION:	-0.950E-02
Y EXPANSION:	0.117E+00

VARIANCES, STANDARD DEVIATIONS

X VARIANCE IS:	0.840E-01
X STD. DEV. IS:	0.290E+00
Y VARIANCE IS:	0.876E-01
Y STD. DEV. IS:	0.296E+00

Figure 1. Vector wafer maps of the local misalignments between the first polysilicon and the contact window levels for wafer 17 made from data obtained using the CBEATS. The length and direction of the line segments at each test site correspond to the vector sum of the measured x- and y-misalignment components. The length scale is given by the bar at lower left indicating the length of a 5-μm misalignment vector. The tabulated results at the lower right give the average x- and y-translation between the two mask levels (in μm), the average angle of rotation (in μrad), the average expansion (in μm per cm), and the variance and standard deviation about the average translation values. a) The initial local misalignment data. b) The remaining local misalignments after the average translation vector is removed. c) The remaining local misalignments after the average translation and rotation vectors are removed. d) The remaining local misalignments after the average translation, rotation, and expansion vectors are removed.



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X ANGULAR CONST:	0.339E+01
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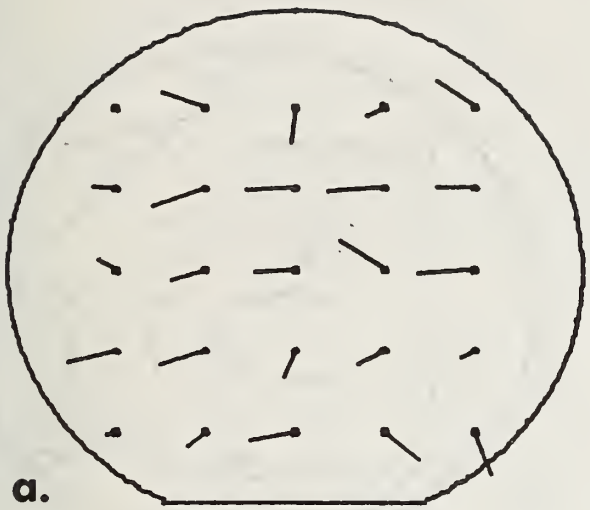
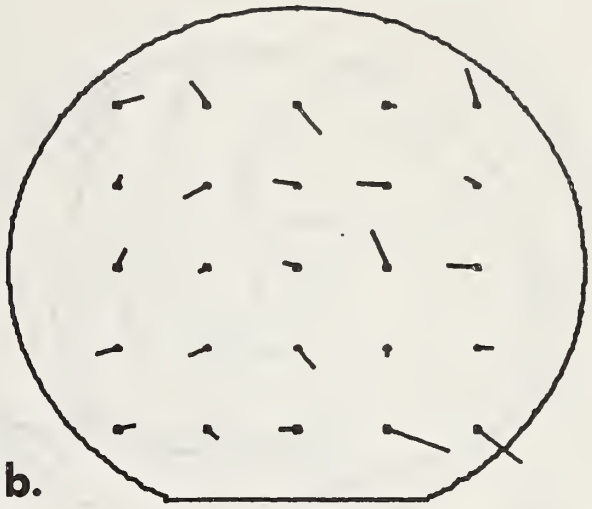
X EXPANSION:	0.179E+00
Y EXPANSION:	0.153E+00

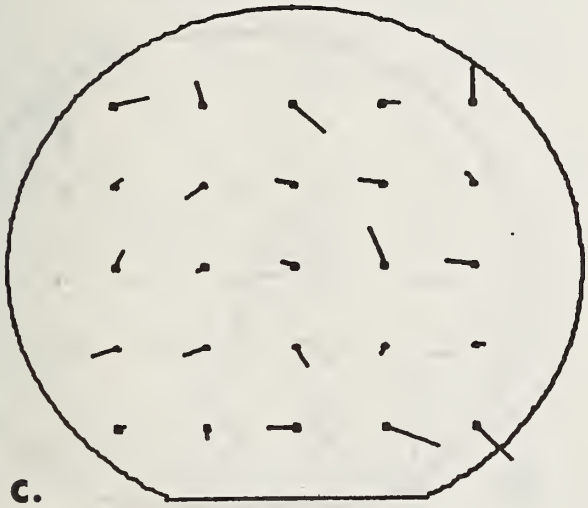
VARIANCES, STANDARD DEVIATIONS

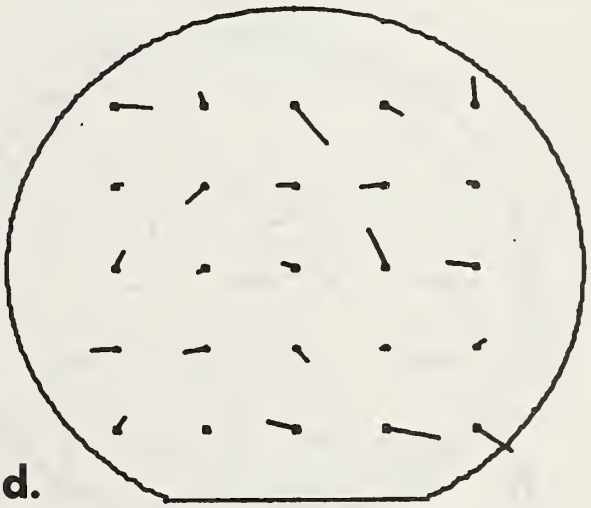
X VARIANCE IS:	0.124E+00
X STD. DEV. IS:	0.353E+00
Y VARIANCE IS:	0.123E+00
Y STD. DEV. IS:	0.351E+00

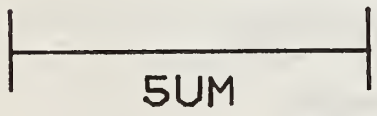
Figure 2. Vector wafer maps of the local misalignments between the second polysilicon and the contact window levels for wafer 17.











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Y ANGULAR CONST:	-0.113E+01
X EXPANSION:	0.385E-02
Y EXPANSION:	0.693E-01

VARIANCES, STANDARD DEVIATIONS

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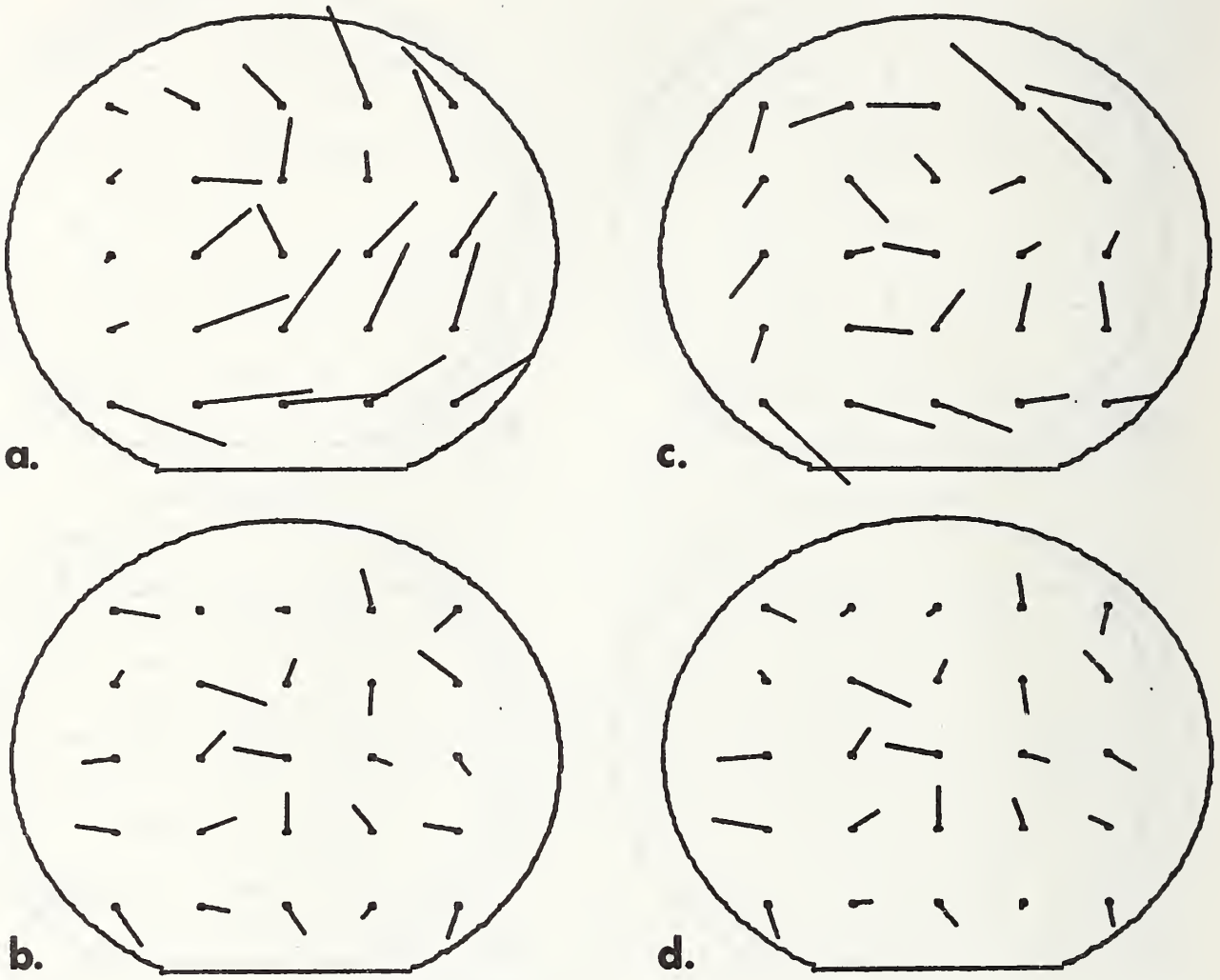
X STD. DEV. IS:	0.329E+00
Y VARIANCE IS:	0.593E-01
Y STD. DEV. IS:	0.244E+00

Figure 3. Vector wafer maps of the local misalignments between the diffusion and the contact window levels for wafer 17.



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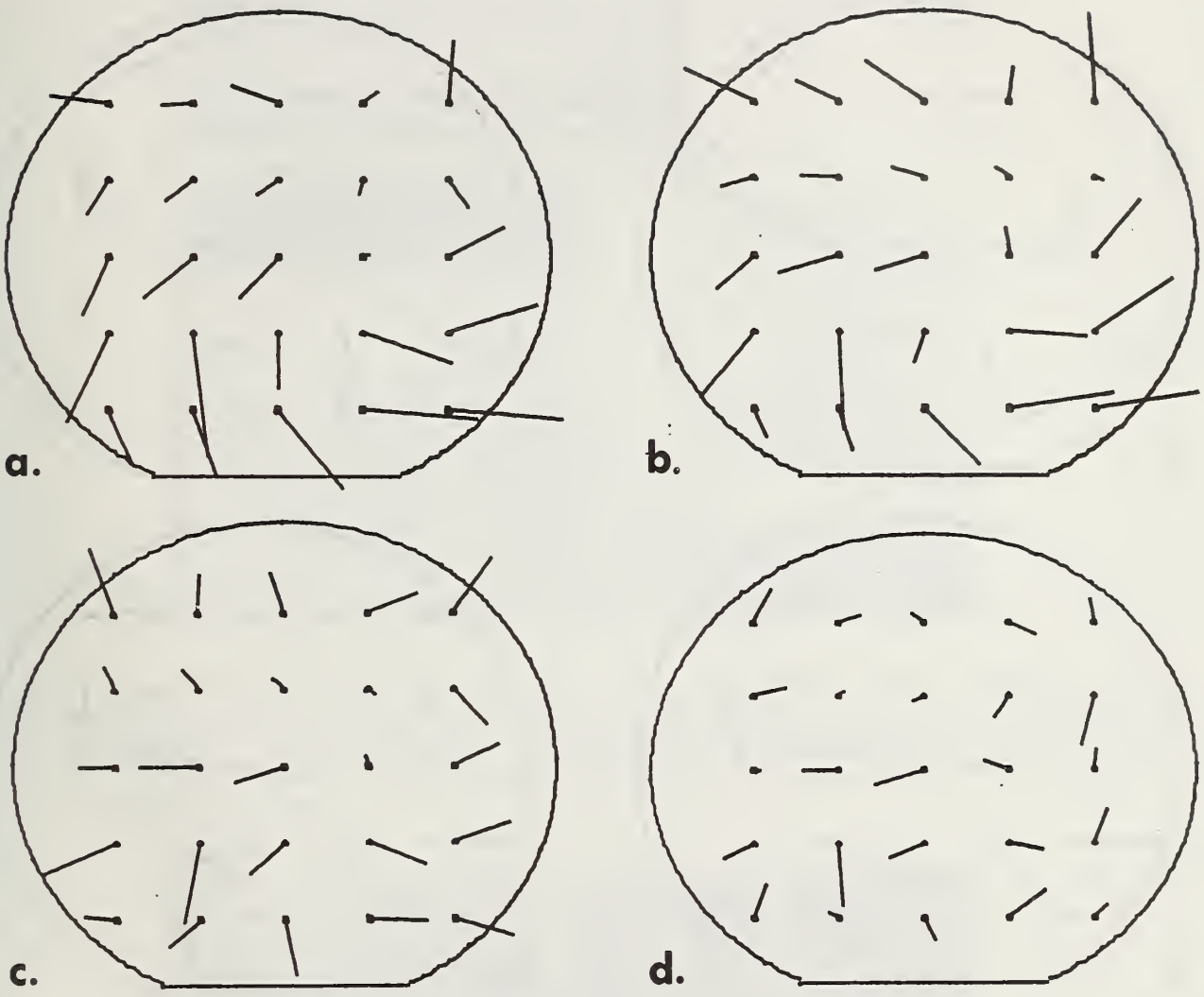
Y ANGULAR CONST:	0.303E+02
X EXPANSION:	-0.102E+00
Y EXPANSION:	0.483E-01

VARIANCES, STANDARD DEVIATIONS

X VARIANCE IS:	0.169E+00
X STD. DEV. IS:	0.411E+00
Y VARIANCE IS:	0.151E+00
Y STD. DEV. IS:	0.389E+00

Figure 4. Vector wafer maps of the local misalignments between the first polysilicon and the contact window levels for wafer 19.



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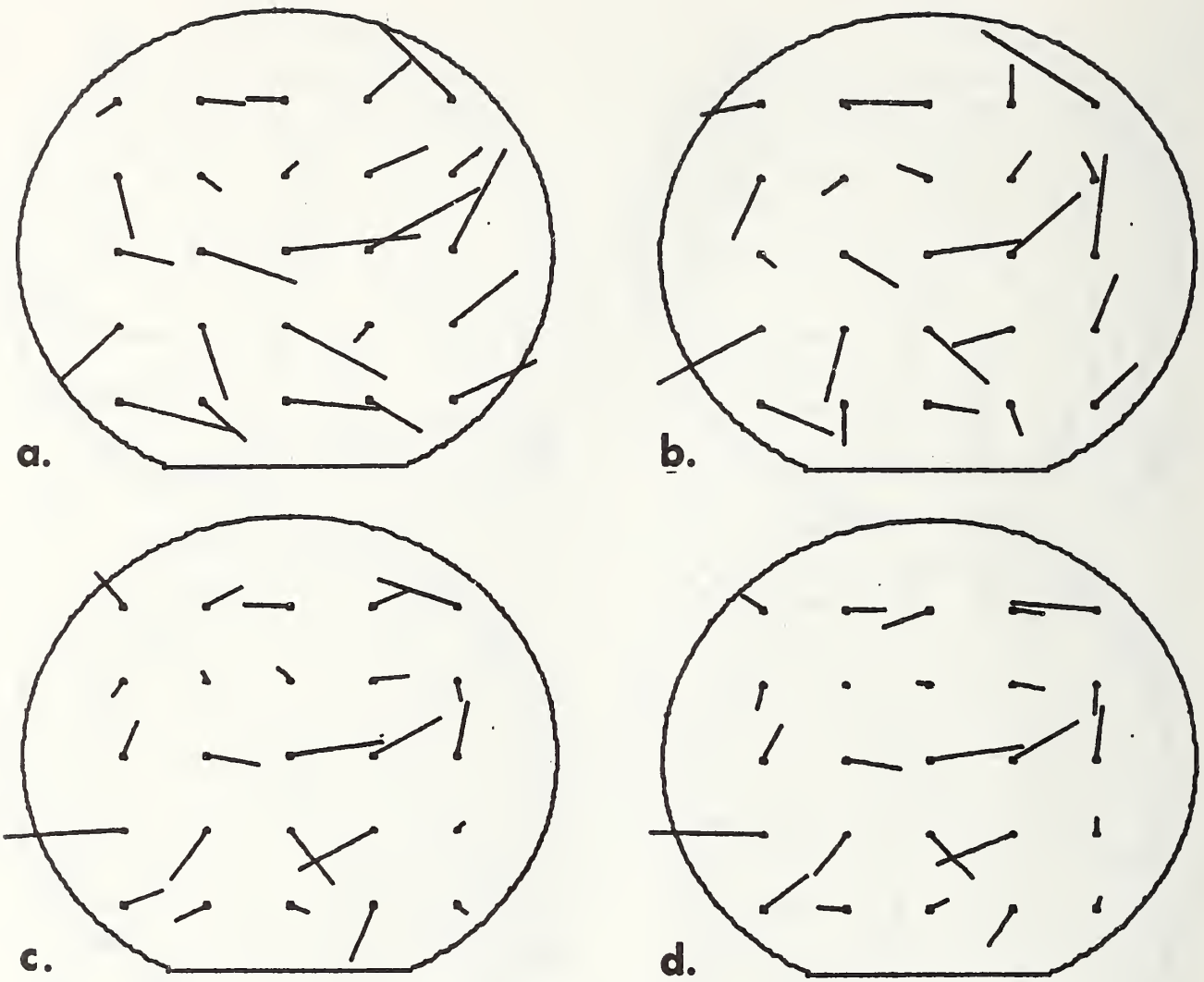
Y ANGULAR CONST:	0.246E+03
X EXPANSION:	0.297E+01
Y EXPANSION:	0.215E+01

VARIANCES, STANDARD DEVIATIONS

X VARIANCE IS:	0.133E+00
X STD. DEV. IS:	0.365E+00
Y VARIANCE IS:	0.181E+00
Y STD. DEV. IS:	0.426E+00

Figure 5. Vector wafer maps of the local misalignments between the second polysilicon and the contact window levels for wafer 19.



X TRANSLATION:	0.623
Y TRANSLATION:	-0.005
X ANGULAR CONST:	0.206E+02
Y ANGULAR CONST:	0.352E+02
X EXPANSION:	0.354E-01
Y EXPANSION:	0.129E+00

VARIANCES, STANDARD DEVIATIONS

X VARIANCE IS:	0.573E+00
X STD. DEV. IS:	0.757E+00
Y VARIANCE IS:	0.190E+00
Y STD. DEV. IS:	0.435E+00

Figure 6. Vector wafer maps of the local misalignments between the diffusion and the contact window levels for wafer 19.

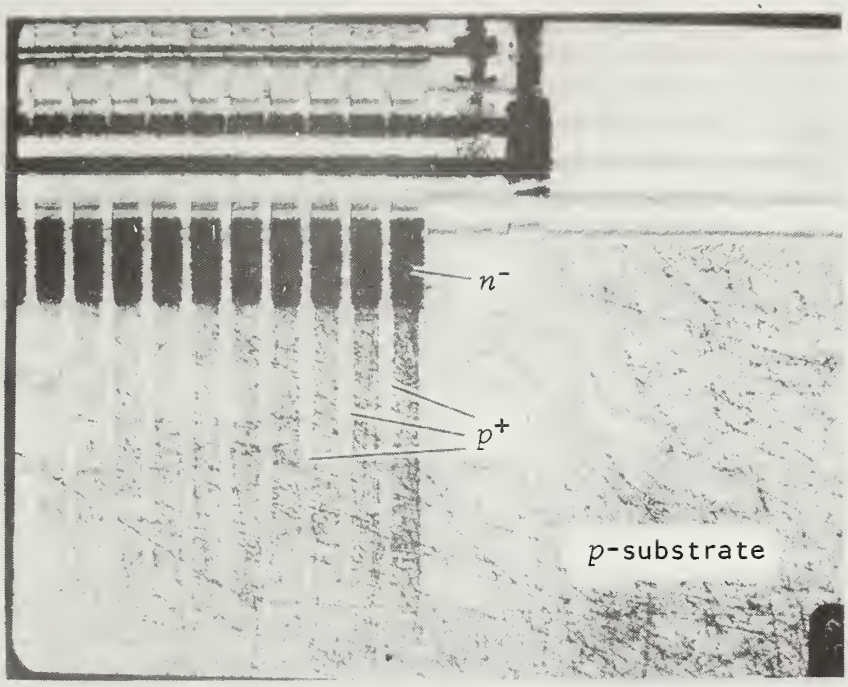


Figure 7. Beveled and stained section of the corner of a CCD. The stain preferentially darkens n-type regions. The n^- buried layer and the p^+ channel stops are identified in the photograph. The magnification in the horizontal direction is 216X. The bevel angle gives approximately 135X additional magnification in the vertical direction.

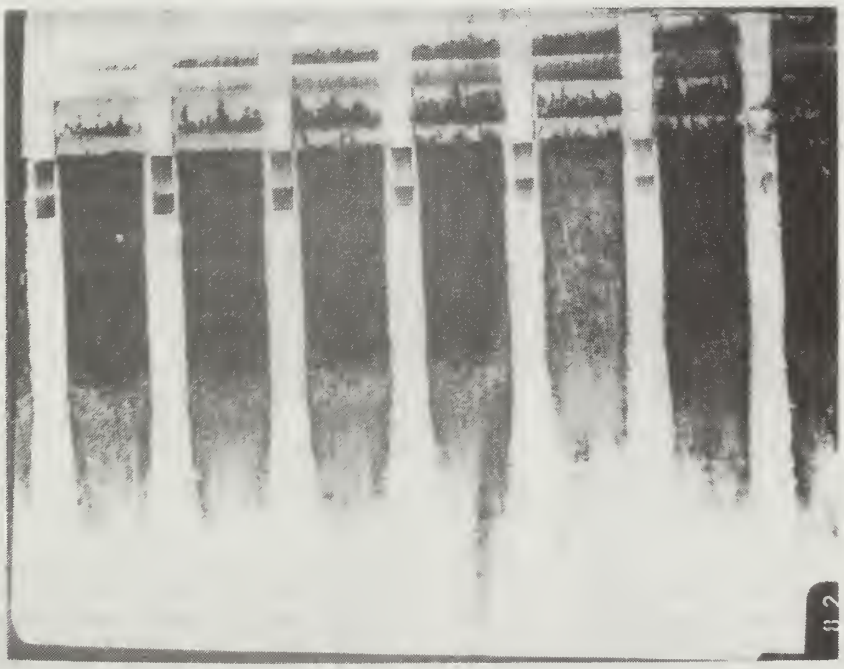


Figure 8. Beveled and stained section of the CCD at higher magnification. The horizontal magnification is approximately 600X.

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5. AUTHOR(S)

G. P. Carver

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

The purpose of this project is to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. During the period covered by this report, consultation was provided to The Charles Stark Draper Laboratory, Inc. (CSDL) and to CSDL contractors on the implementation and use of test structures developed previously during this project. In addition, the results of measurements on CCD imager wafers using the surface-channel and buried-channel, integrated gated-diode electrometers, before and after exposure to ^{60}Co radiation, and using the cross bridge/electrical alignment test structures are reported. Examples of cross sections of the CCDs made by beveling and staining are also presented.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

CCD; cross-bridge sheet resistor; electrical alignment test structure; gated diode; integrated gated-diode electrometer; integrated test structure; MOSFET dc profiler; test structure.

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